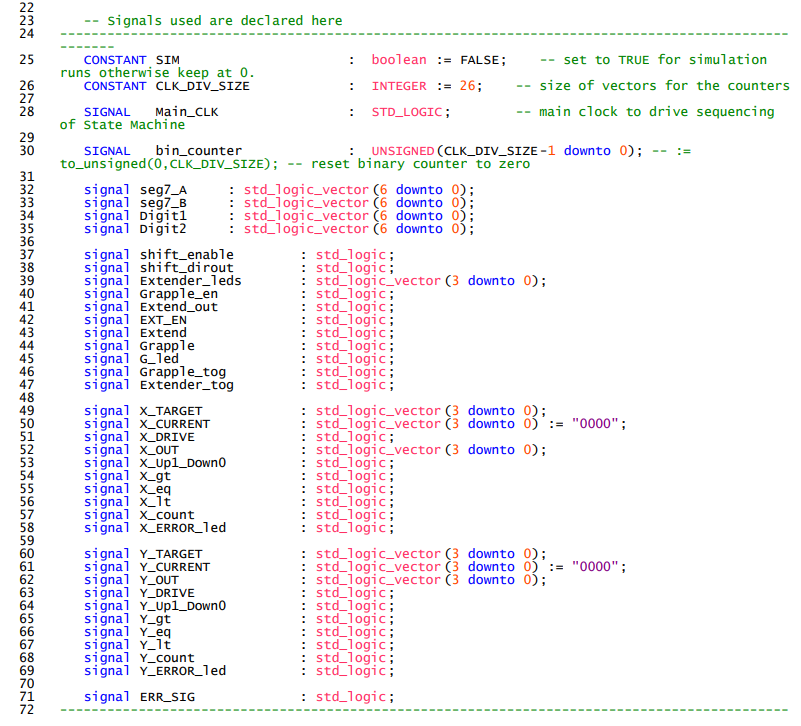
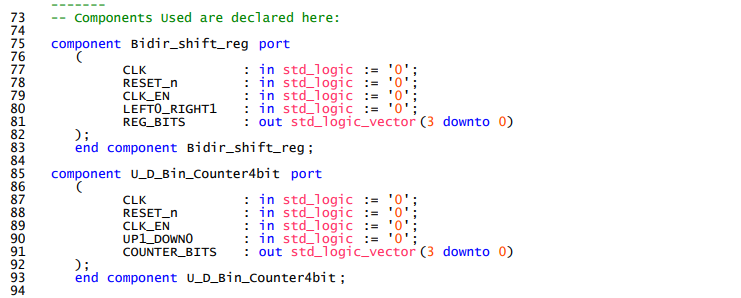
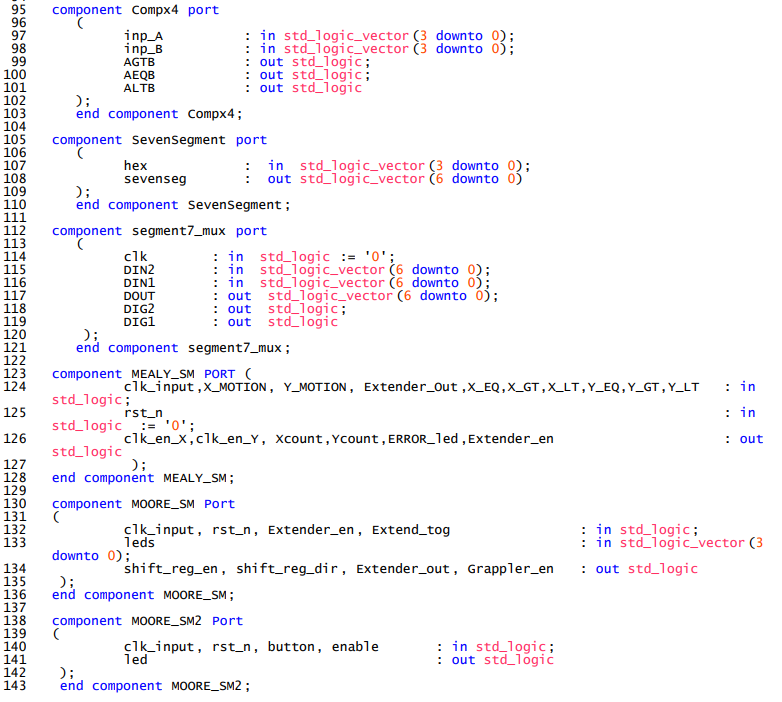
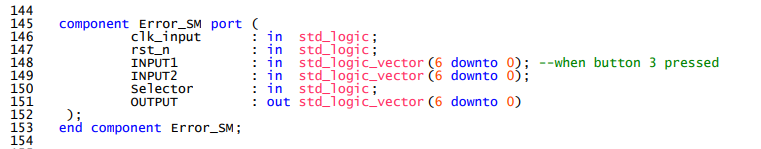
**Lab 4 Group 12 Session 205 Report**

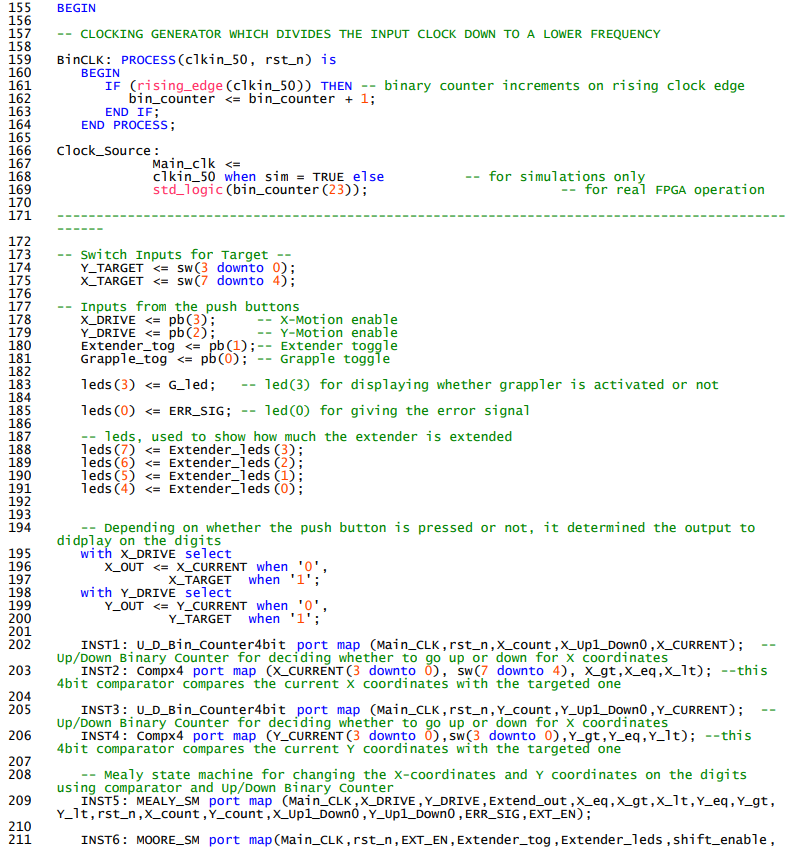
**Part 1**: LogicalStep\_Lab4\_top.vhd File

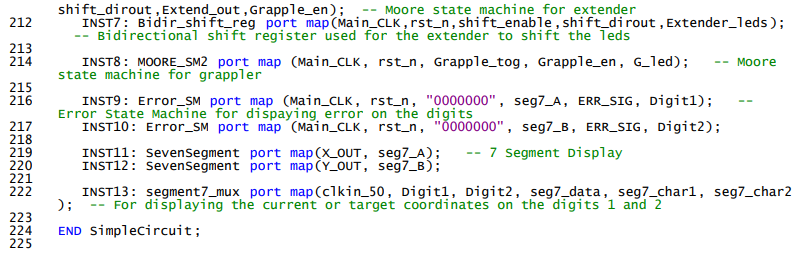












**Part 2**: Simulations of 8bit Shift Register and 8bit Binary Counter

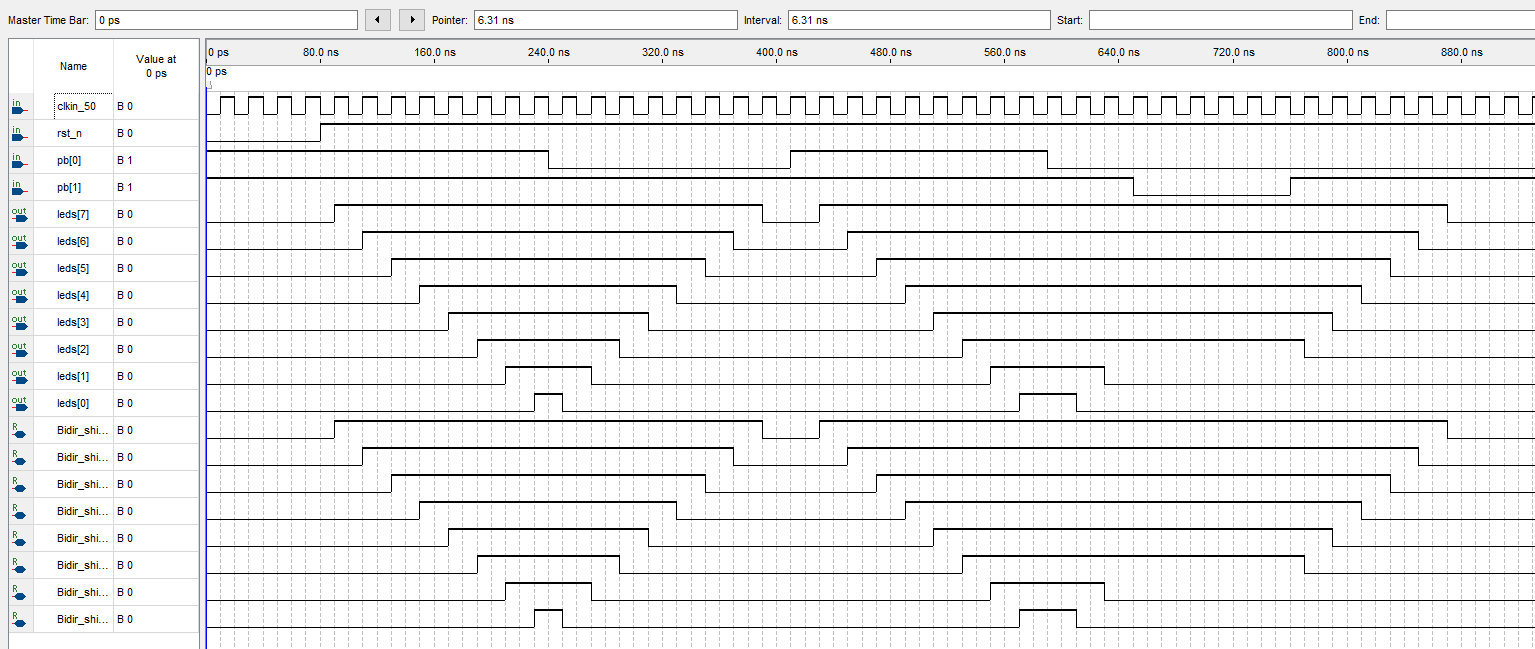


Figure1: Simulation of 8bit Shift Register

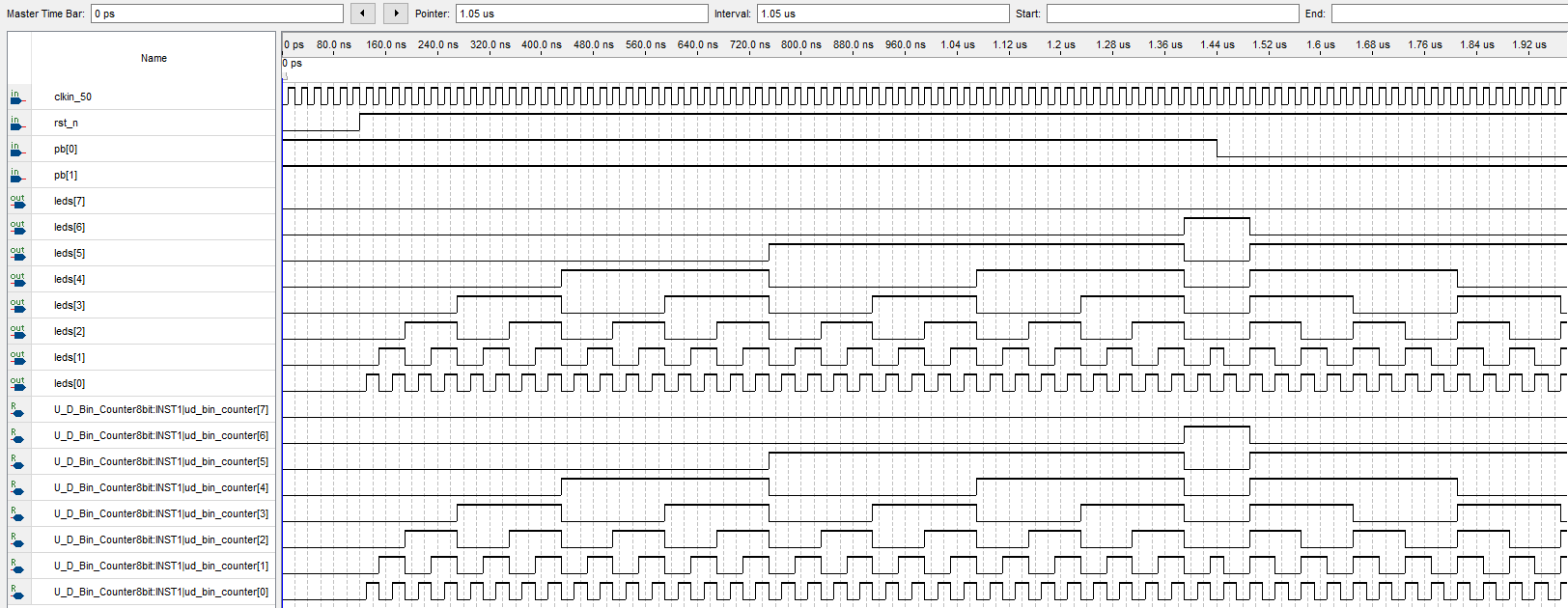


Figure1: Simulation of 8bit Binary Counter

**Part 3:** State Diagrams of Mealy State Machine and Moore State Machine 1

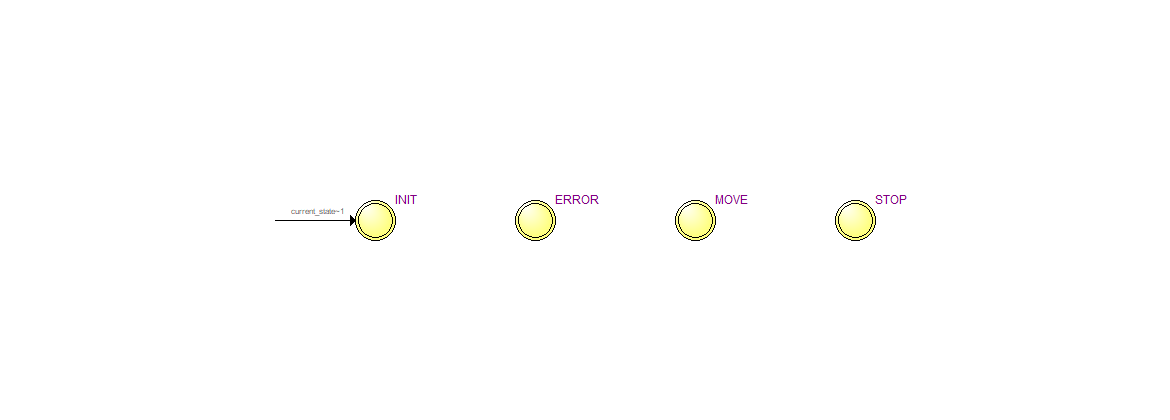


Figure1: State Diagram of Mealy State Machine

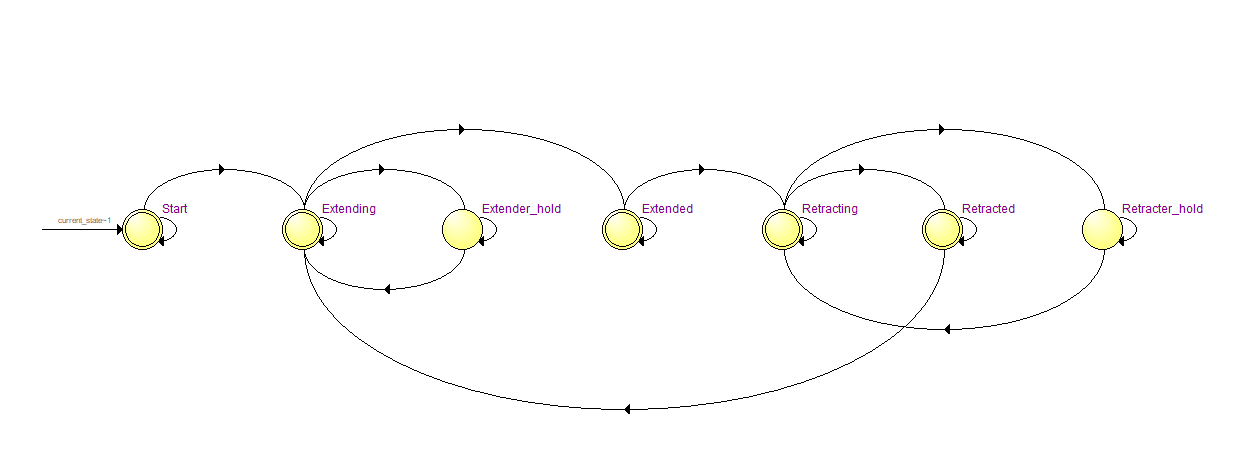
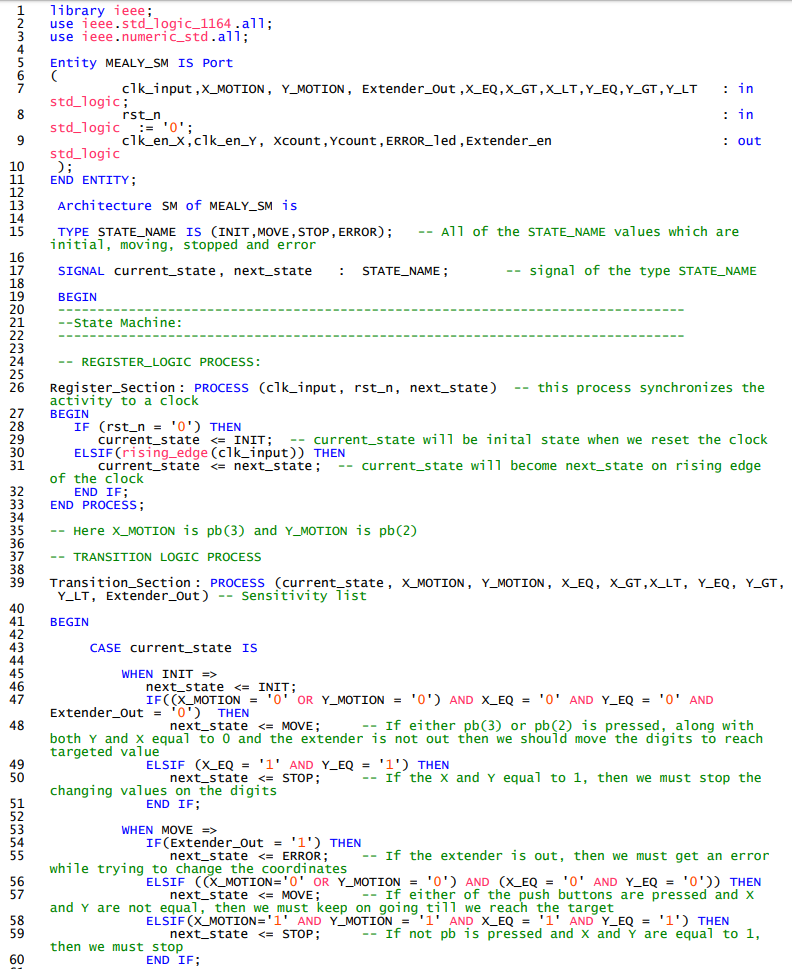


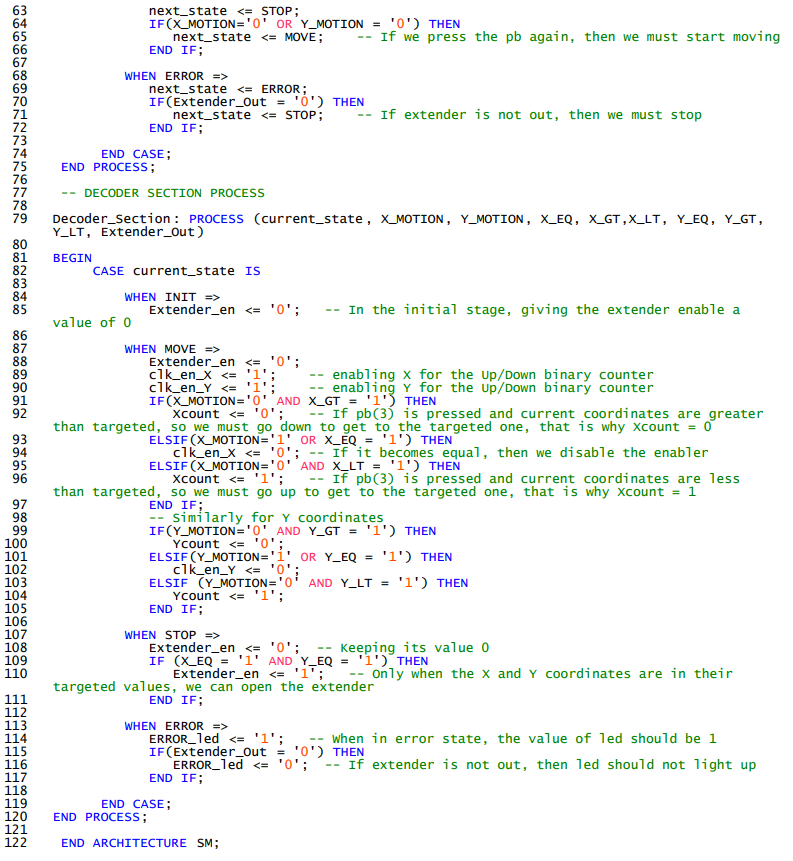
Figure2: State Diagram of Moore SM1

**Part 4:** Mealy form Mealy SM and Moore form of Moore SM1

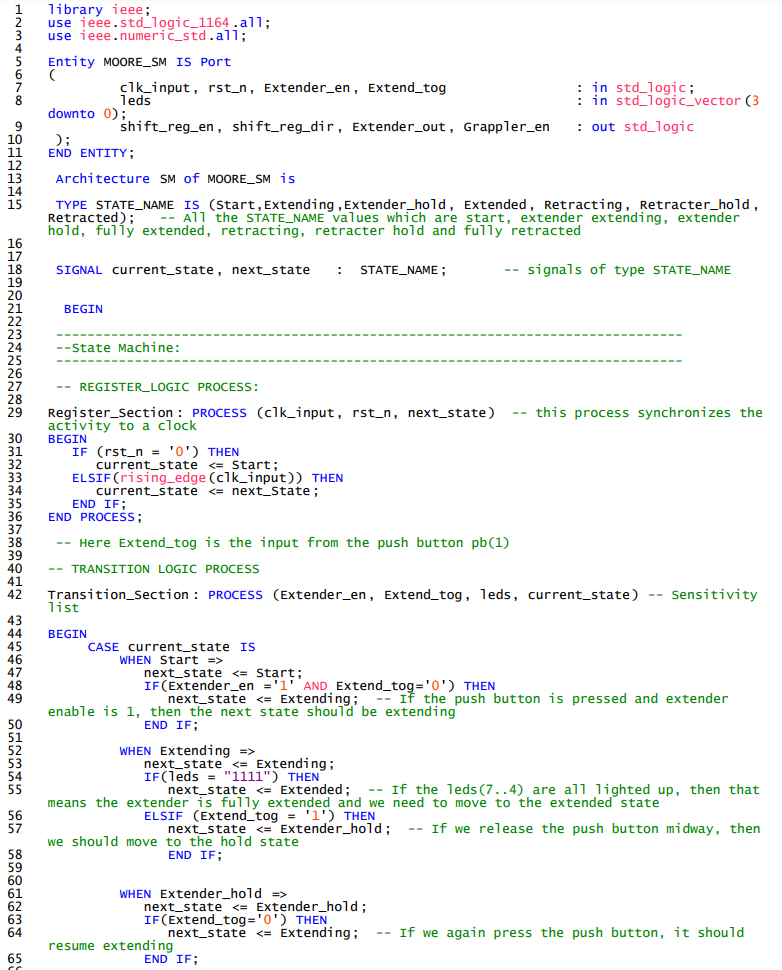
1. Mealy SM:



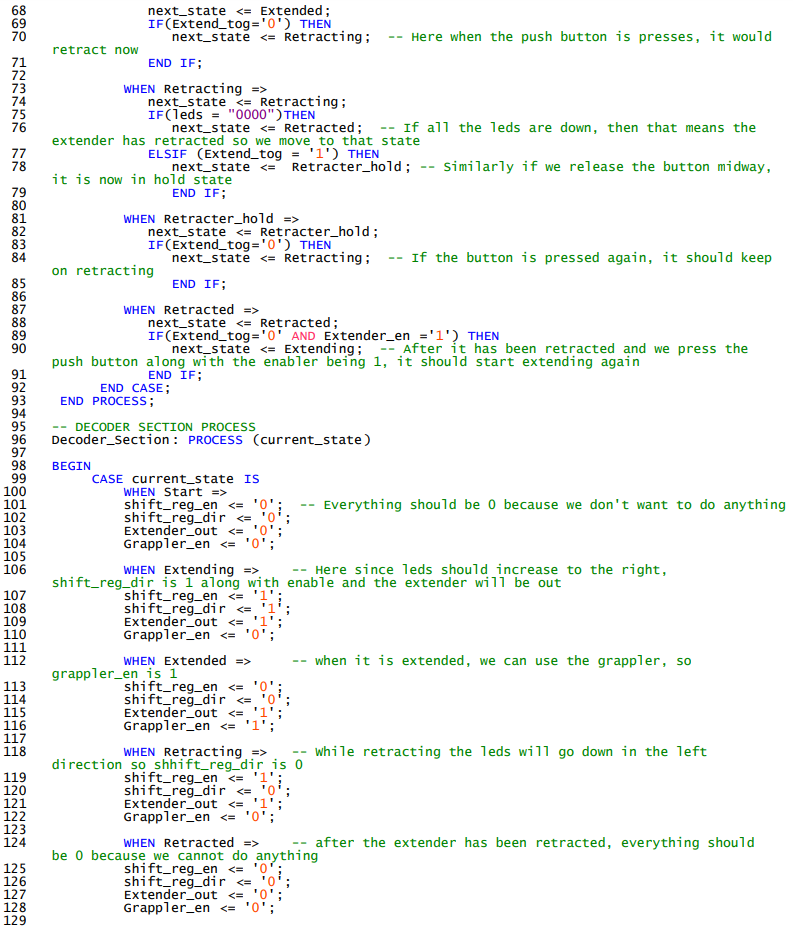


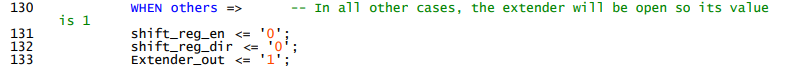


1. Moore SM1:







**Part 5:** Fitter Report on Resource Utilization by Entity

